Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 034299-688	Serial No. 10/574,315
Information Disclosure Statement by Applicant	Applicant: Mickael Guibert et al.	
(Use several sheets if necessary)	Filed: March 30, 2005	Group: (to be assigned)

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
VTa	A	5,892,962	04/06/99	Cloutier			
VTa	B	6,150,839	11/21/00	New et al.			

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

VTa	C	Altera, "Flex 8000 Programmable Logic Device Family", pages 361-363 (June 1999)
VTa	D	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing", Ph.D. Thesis, MIT (Abstract), 368 pages (August 1996)
VTa	E	Fujii, Taro, et al., "A Dynamically Reconfigurable Logic Engine With a Multi-Context/Multi-Mode Unified-Cell Architecture", *IEEE International Solid-State Circuits Conference*, pages 364-365, page 479 (Feb 1999)
VTa	F	Goldstein, S. Copen, et al., "PipeRench: A Reconfigurable Architecture and Compiler", in *IEEE Computer*, Vol. 33, No. 4, pages 70-77 (April 2000)
VTa	G	John, L. K. et al., "A Dynamically Reconfigurable Interconnect For Array Processors", ieee Transactions on Very Large Scale Integration (VLSI) Systems", *IEEE, INC.*, Vol. 6, No. 1, pages 150-157 - 03/1998
VTa	H	Levine, Benjamin A., et al., "PipeRench: Power and Performance Evaluation of a Programmable Pipelined Datapath", Hot Chips 14, Palo Alto, CA (August 2002)
VTa	I	Sassatelli, G., et al., "Highly Scalable Dynamically Reconfigurable Systolic Ring-Architecture for DSP Applications", *PROCEEDINGS DESING, AUTOMATION AND TEST IN EUROPE* (March 2002)
VTa	J	Tau, Edward, et al., "A First Generation DPGA Implementation", in proceedings of the Third Canadian Workshop on Field-Programmable Devices, pages 138-143 (May 1995)
VTa	K	JTAG; Test Technology Standards Committee "IEEE Std. 1149.1 Standard Test Access Port and Boundry-Scan Architecture", Institute of Electrical and Electronics Engineers (October 1993)

Examiner	Date Considered 4/23/07

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.